What is Claimed:

1. A bandpass delta sigma truncator comprising:

input means for receiving a series of first multi-bit digital signals each having:

(a) a number of data bits, and

(b) a first number of sign bits;

sign extending means for sign extending each of the first multi-bit digital signals to a second multi-bit digital signal having:

(a) the same number of data bits as the number of data bits in the first multi-bit digital signals, and

(b) a second number of sign bits;

output means for supplying from a series of third multi-bit digital signals each individually associated with one of the second multi-bit digital signals and each having the same number of data bits as in an associated second multi-bit digital signal:

(a) a series of fourth multi-bit digital signals each having a selected number of the most significant data bits of the third multi-bit digital signals, and

(b) a series of fifth multi-bit digital signals each having the remaining number of the least significant data bits of the third multi-bit digital signals;

means for:

(a) delaying by a period of time equal to the time between successive first multi-bit digital signals each of the fifth multi-bit digital signals, and

(b) delaying by a period of time equal to twice the time between successive first multi-bit digital signals each of the fifth multi-bit digital signals and inverting the fifth multi-bit digital signals that have been delayed by a period of time equal to twice the time between successive first multi-bit digital signals;

means for multiplying by a multiplier number related to the ratio of a selected frequency to the frequency of the first multi-bit digital signals each of the fifth multi-bit digital signals delayed by a period of time equal to the time between successive first multi-bit digital signals and developing a series of sixth

multi-bit digital signals having a number of data bits that is the product of the multiplier number and the number of data bits in the fifth multi-bit digital signals; and

summing means for adding to each second multi-bit digital signal:

(a) a fifth multi-bit digital signal that has been delayed by a period of time equal to twice the time between successive first multi-bit digital signals and inverted, and

(b) a sixth multi-bit digital signal

to develop the series of third multi-bit digital signals.

2. A bandpass delta sigma truncator according to claim 1 wherein:

(a) each first multi-bit digital signal is a ten bit digital signal having nine data bits and one sign bit,

(b) each second multi-bit digital signal is an eleven bit digital signal having nine data bits and two sign bits,

(c) each third multi-bit digital signal is a nine bit digital signal having nine data bits,

(d) each fourth multi-bit digital signal is a six bit digital signal having six data bits,

(e) each fifth multi-bit digital signal is a three bit digital signal having three data bits,

(f) each sixth multi-bit digital signal is a four bit digital signal having four data bits,

(g) the multiplier number is 1.75,

(h) the selected frequency is 5MHZ, and

(i) the frequency of the first multi-bit digital signals is 30MHZ.

3. A bandpass delta sigma truncator according to claim 1 further including means between said summing means and said output means for determining whether the value of any third multi-bit digital signal is one of:

(a) greater than a first value, and

(b) less than a second value.

4. A bandpass delta sigma truncator according to claim 2 further including means between said summing means and said output means for determining whether the value of any third multi-bit digital signal is one of:

(a) greater than a first value, and

(b) less than a second value.

5. A bandpass delta sigma truncator according to claim 2 wherein said means for delaying and inverting the fifth multi-bit digital signals include:

(a) a digital delay circuit for delaying by a period of time equal to the time between successive first multi-bit digital signals each of the fifth multi-bit digital signals, and

(b) a digital delay and inverter circuit for:

(1) additionally delaying by a period of time equal to the time between successive first multi-bit digital signals each of the fifth multi-bit digital signals delayed by said digital delay circuit, and

(2) inverting the additionally delayed fifth multi-bit digital signals.

6. A bandpass delta sigma truncator according to claim 4 wherein said means for delaying and inverting the fifth multi-bit digital signals include:

(a) a digital delay circuit for delaying by a period of time equal to the time between successive first multi-bit digital signals each of the fifth multi-bit digital signals, and

(b) a digital delay and inverter circuit for:

(1) additionally delaying by a period of time equal to the time between successive first multi-bit digital signals each of the fifth multi-bit digital signals delayed by said digital delay circuit, and

(2) inverting the additionally delayed fifth multi-bit digital signals.

7. A method for truncating a multi-bit digital signal comprising the steps of:

providing a series of first multi-bit digital signals each having:

(a) a number of data bits, and

(b) a first number of sign bits;

sign extending each of the first multi-bit digital signals to a second multi-bit digital signal having:

(a) the same number of data bits as the number of data bits in the first multi-bit digital signals, and

(b) a second number of sign bits;

adding to each second multi-bit digital signal to develop a series of third multi-bit digital signals each individually associated with one of the second multi-bit digital signals and each having the same number of data bits as in an associated second multi-bit digital signal:

(a) a multi-bit digital signal that has been:

(1) developed from a selected number of the least significant bits of the third multi-bit digital signals, and

(2) delayed by a period of time equal to twice the time between successive first multi-bit digital signals and inverted, and

(b) a multi-bit digital signal that has been:

(1) developed from the selected number of the least significant bits of the third multi-bit digital signals, and

(2) delayed by a period of time equal to the time between successive first multi-bit digital signals and multiplied by a multiplier number related to the ratio of a selected frequency to the frequency of the first multi-bit digital signals; and.

developing from the third multi-bit digital signals a series of fourth digital signals each having a selected number of the most significant data bits of the third multi-bit digital signals.

8. A method for truncating a multi-bit digital signal according to claim 7 wherein:

(a) each first multi-bit digital signal is a ten bit digital signal having nine data bits and one sign bit,

(b) each second multi-bit digital signal is an eleven bit digital signal having nine data bits and two sign bits,

(c) each third multi-bit digital signal is a nine bit digital signal having nine data bits,

(d) each fourth multi-bit digital signal is a six bit digital signal having six data bits,

(e) each multi-bit digital signal that has been delayed by a period of time equal to twice the time between successive

first multi-bit digital signals and inverted is a three bit digital signal having three data bits,

(f) each multi-bit digital signal delayed by a period of time equal to the time between successive first multi-bit digital signals and multiplied by a multiplier number related to the ratio of a selected frequency to the frequency of the first multi-bit digital signals is a four bit digital signal having four data bits,

(g) the multiplier number is 1.75,

(h) the selected frequency is 5MHZ, and

(i) the frequency of the first multi-bit digital signals is 30MHZ.

9. A method for truncating a multi-bit digital signal according to claim 7 further including the step of determining whether the value of any third multi-bit digital signal is one of:

(a) greater than a first value, and

(b) less than a second value.

10. A method for truncating a multi-bit digital signal according to claim 8 further including the step of determining whether the value of any third multi-bit digital signal is one of:

(a) greater than a first value, and

(b) less than a second value.